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TITLE OF THE INVENTION:

A METHOD, SYSTEM, AND APPARATUS FOR SUPPORTING POWER LOSS RECOVERY IN ECC ENABLED MEMORY DEVICES

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BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates generally to supporting Error Correcting Code (ECC) enabled memory devices, specifically, a novel mechanism for a Power Loss Recovery (PLR) algorithm and flash media format for flash media management software.

Description of the Related Art

The demand for quicker and more powerful communication devices has led to many technological advances, including flash memory and the ability to store and retain data despite the loss of power. A non-volatile memory has the ability to retain the data despite loss of power and is one of the enabling technologies for the wireless and cellular revolution.

A flash media is a system with various configurations of flash memory devices to create a non-volatile storage. One example is a system with a 32 bit bus and multiple 8 bit flash memory devices coupled to the 32 bit bus. Also, flash media could be hardware with additional decoding logic to manage and coordinate the various arrays of flash memory devices. Thus, the flash media exhibits the same flash memory device read, program, and erase characteristics. A flash media could be coupled to a file system, which has the interface and logic to manage files and directories. Thus, the interface with the file system allows for the ability to create, delete, move, read, write, and flush files and create, get, delete, read, flush, and write directories.

Typically, a flash media management software divides a flash memory block into individual data units or sectors, wherein each sector has an associated header for identifying a sector's status. Likewise, status bits or paired bits in Multi-Level Cell (MLC) flash are utilized for tracking the current state of each sector. However, as depicted in Figure 1, the prior art flash media format interleaves the PLR status tracking information with the data units. However, an

ECC enabled flash memory device might have an entire block of data unprotected by the ECC. Typically, ECC is similar to parity because additional bits of information are added to data for detecting and correcting individual bit errors. For example, a single bit error may result in a complete inverse of the ECC parity. Typically, the data may be changed to correct the single bit error. However, for an ECC enabled flash memory device that stores the ECC information, one needs to invalidate the ECC because of the single bit error. Based on Figure 2, this may result in data that is unprotected because of the interleaving of PLR status bits with the data.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the following figures. Like references indicate similar elements, in which:

Figures 1 and 2 depict the prior art.

Fig. 3 shows a format of bits in accordance with one embodiment.

Fig. 4 shows a table for status bits in accordance with one embodiment.

Fig. 5 shows a flowchart of a method in accordance with one embodiment.

Fig. 6 shows a system in accordance with one embodiment.

DETAILED DESCRIPTION OF THE INVENTION

A method, system and apparatus for supporting ECC enabled memory devices in flash media systems is discussed. In the following description, for purposes of explanation, numerous details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that these specific details are not required in order to practice the present invention.

As previously described, a problem exists for current flash media formats that interleave PLR status bits with data and may result in data that is unprotected because of the interleaving of PLR status bits with the data. In contrast, the claimed subject matter proposes a novel technique for rearranging the PLR status bits such that all the status bits are extracted from the header and data area and united (coalesced) into a predetermined region. Thus, this rearranged PLR status bits allows the PLR status bits to be updated without invalidating the ECC and results in protecting the data.

Fig. 3 shows a format of bits in accordance with one embodiment. As previously described, a flash media management software divides a flash memory block into individual data units or sectors, wherein each sector has an associated header for identifying a sector's status. Likewise, status bits or paired bits in Multi-Level Cell (MLC) flash are utilized for tracking the current state of each sector. In contrast to the prior art, the claimed subject matter as depicted in Figure 3, depicts a novel technique for rearranging the PLR status bits such that all the status bits are extracted from the header and data area and united (coalesced) into a predetermined region. For example, the PLR coalesced region 302 contains all the PLR status bits and is associated with individual headers 304, 306, and 308. Each header 304, 306, and 308 are associated for one of the fragment data sections. The PLR status bits do not need the ECC protection, which will be

discussed further in connection with Figure 4. Thus, this rearranged PLR status bits allows the PLR status bits to be updated without invalidating the ECC and results in protecting the data. In contrast, the prior art did not offer the ECC protection to the data because of the issue with PLR status tracking bit updates that was previously described.

The fragment data units will receive full ECC protection because they are written to in a single time

In one embodiment, the apparatus of Figure 3 is incorporated within an ECC enabled flash memory device. Also, in another embodiment, the apparatus is supervised by flash media management software to support and partition the ECC enabled flash memory devices.

Fig. 4 shows a table for status bits in accordance with one embodiment. In one embodiment, the claimed subject matter of Figure 4 depicts multi level states 402 in a MLC flash that are utilized for PLR status bits. For example, in this embodiment, the ECC scheme is designed to protect against bit errors in the intermediate MLC states, such as, Levels 2 (1,0) and Level 3 (0,1). As depicted in 404, the Levels 2 and 3 are in the middle of the Vt graph. In contrast, the Levels 1(1,1) and 4 (0,0) are at opposite ends of the Vt graph and have the biggest difference in Vt, wherein Vt is a voltage threshold between levels. Therefore, for one embodiment, the PLR status tracking bits deploy Levels 1 and Level 4 states. Furthermore, levels 1 and 4 are the lowest Vt level and highest Vt level for this embodiment.

Figure 5 depicts a flowchart for a method in accordance with one embodiment. For example, the flowchart depicts a novel method for coalescing PLR status bits , into a predetermined region, as depicted in a block 502. Likewise, each PLR status bit may be programmed to have one of a plurality of MLC levels, as depicted in a block 504. In one

embodiment, each PLR status bit may have either the highest Vt level or the lowest Vt level. Consequently, in one embodiment, the claimed subject matter allows for ignoring the ECC scheme for the PLR status bits because it was designed to protect for bit errors for intermediate Vt levels.

In one embodiment, the flowchart is implemented in a flash media management software to support and partition the ECC enabled flash memory devices.

Fig. 6 shows a system in accordance with one embodiment. In one embodiment, the system 600 has a wireless interface. The system comprises a microprocessor 610 coupled to an internal bus 620. Likewise, the system comprises a peripheral bus interface 550, a digital signal processor (dsp) 630, and a flash memory 640 coupled to the internal bus 620. Finally, a wireless interface 670 is coupled an antenna 680 and the bus interface 650. The wireless interface receives and transmits data and information. Also, the microprocessor and dsp perform calculations and operations involving searches of the flash memory via the internal bus 620.

In one embodiment, the system incorporates the method and apparatus depicted earlier in connection with Figures 3-5.

Although the invention has been described with reference to specific embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the disclosed embodiment, as well as alternative embodiments of the invention, will become apparent to persons skilled in the art upon reference to the description of the invention. It is contemplated, therefore, that such modifications can be made without departing from the spirit or scope of the present invention as defined in the appended claims.